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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,805	12/07/2001	Hiromasa Shimizu	HITA.0131	7667
38327 7.	590 11/16/2005		EXAMINER	
REED SMITE		SEFER, AHMED N		
3110 FAIRVIEW PARK DRIVE, SUITE 1400 FALLS CHURCH, VA 22042		ART UNIT	PAPER NUMBER	
			2826	
				5

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)					
Office Action Commence	10/004,805	SHIMIZU ET AL.	(PM)				
Office Action Summary	Examiner	Art Unit					
	A. Sefer	2826	,				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence add	tress				
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 6(a). In no event, however, may a reply be tim ill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE!	N. nely filed the mailing date of this co D (35 U.S.C. § 133).					
Status							
1) Responsive to communication(s) filed on 01 Se	eptember 2005.						
	action is non-final.						
3) Since this application is in condition for allowan	•	secution as to the	merits is				
closed in accordance with the practice under E	· ·						
Disposition of Claims							
4) Claim(s) <u>1,6,8,9 and 12-15</u> is/are pending in the	annlication						
4a) Of the above claim(s) is/are withdraw	• •						
5) Claim(s) is/are allowed.	in nom consideration.						
6)⊠ Claim(s) <u>1,6,8,9 and 12-15</u> is/are rejected.							
7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/or	election requirement						
or oralling) are subject to restriction and/or	election requirement.	•					
Application Papers							
9) The specification is objected to by the Examiner							
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.							
Applicant may not request that any objection to the d	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction	on is required if the drawing(s) is obj	ected to. See 37 CF	R 1.121(d).				
11)☐ The oath or declaration is objected to by the Exa	aminer. Note the attached Office	Action or form PT0	O-152.				
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:	priority under 35 U.S.C. § 119(a)	-(d) or (f).					
1. Certified copies of the priority documents	have been received.						
2. Certified copies of the priority documents	have been received in Application	on No					
3. Copies of the certified copies of the priori			Stage				
application from the International Bureau	(PCT Rule 17.2(a)).		-				
* See the attached detailed Office action for a list of	of the certified copies not receive	d.					
·							
Attachment(s)							
1) Motice of References Cited (PTO-892) 4) Interview Summary (PTO-413)							
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Notice of Informal Patent Application (PTO-152)							
B) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	6) Other:	atent Application (PTO-	102)				

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/1/2005 has been entered.

Claim Objections

2. Claim 13 is objected to because of the following informalities: In lines 12 and 15 of claim 13, the recitation calling for "... between neighboring pixel regions ..." should read "... between said neighboring pixel regions ...". Appropriate correction is required.

Allowable Subject Matter

3. The indicated allowability of claim 1 is withdrawn in view of the newly discovered reference(s) to Suzuki ("Suzuki") JP 11-142863 (see also equivalent US PG-Pub 2002/0008834). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 6, 9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki.

Suzuki discloses in figs. 1 and 2 a liquid crystal display device comprising a first substrate on a main surface thereof, a black mask 24 and color filters 21-23, each arranged in an aperture of the black mask, being formed; a liquid crystal layer L; a second substrate 1 disposed opposite to the first substrate across the liquid crystal layer and stuck to the first substrate by a sealing material (not shown) applied to the peripheries of a main surface of the first substrate facing the liquid crystal layer and of a main surface of the second substrate facing the liquid crystal; a stacked structure formed on the main surface of the second substrate by stacking in order first signal lines 10/11, an insulating film 15 covering the first signal lines, and second signal lines 12/13 each overlappingly intersecting the first signal lines over the insulating film therebetween; a plurality of pixel regions 18 formed as being surrounded by respective neighboring first signal lines and second signal lines first on the second substrate; and first spacers 31 and second spacers 30 both formed on the main surfaces of the first substrate, and arranged corresponding to portions of the stacked structure located between neighboring pixel regions and the liquid crystal layer, wherein each of second spacers being ordinarily spaced from the stacked structure formed on the second substrate to accommodate the liquid crystal layer therebetween, and each of the first spacers ordinarily contacting directly with the stacked structure formed on the second substrate, wherein some of said portions of the stacked structure contacting with the first spacers are thicker than others of said portions of the stacked structure corresponding to the second spacers with the liquid crystal layer interposed therebetween.

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Regarding claim 6, Suzuki discloses each of the second spacers contacts with the stacked structure formed on the second substrate while the first spacers be subjected to an external force.

Regarding claim 9, Suzuki discloses the black mask and the color filters being covered by a protective film 25, and the first spacers and the second spacers being formed on top of the protective film.

Regarding claim 12, Suzuki discloses a second substrate having a plurality of pixels (not shown) arranged on the main surface thereof, and each of the pixels has a switching element controlled by one of the first signal lines and a pixel electrode receiving a signal from one of the second signal lines through the switching element.

6. Claims 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki.

Suzuki discloses in figs. 1 and 2 a liquid crystal display device comprising: a first substrate 2 including color filters 21-23; a liquid crystal layer L; a second substrate 1 disposed opposite to the first substrate across the liquid crystal layer; first signal lines 10/11 formed on the second substrate; second signal lines 12/13 intersecting the first signal lines with an insulating film provided therebetween; a plurality of pixel regions 18 formed as being surrounded by respective neighboring first signal lines and second signal lines; a base pattern 20 formed between neighboring pixel regions; a plurality of first spacers 31 formed above a main surface of the first substrate and arranged above a part where is between neighboring pixel regions and overlaps with the base pattern in a plan view, wherein a plurality of second spacers 30 formed on the main surface of the first substrate and arranged above a part where is between neighboring pixel regions and doe not overlap with the base pattern in a plan view, wherein each of the second spacers is ordinarily spaced from a stacked structure formed on the second

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substrate to accommodate the liquid crystal layer therebetween, and each of the first spacers ordinarily contacts directly the stacked structure formed on the second substrate.

Regarding claim 14, Suzuki discloses each of the second spacers contacts with the stacked structure formed on the second substrate, when the first spacers are subjected to an external force and elastically deformed.

Regarding claim 15, Suzuki discloses the base pattern is covered by a protective film 25 provided between the base pattern and the first spacers.

7. Claims 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Sumida ("Sumida") (of record) JP 2000-75281.

Sumida discloses in fig. 2 a liquid crystal display device comprising: a first substrate 91 including color filters 31-33; a liquid crystal layer 6; a second substrate 92 disposed opposite to the first substrate across the liquid crystal layer; first signal lines (unnumbered) formed on the second substrate; second signal lines (unnumbered) intersecting the first signal lines with an insulating film provided therebetween; a plurality of pixel regions formed as being surrounded by respective neighboring first signal lines and second signal lines; a base pattern 2 formed between neighboring pixel regions; a plurality of first spacers 7 formed above a main surface of the first substrate and arranged above a part where is between neighboring pixel regions and overlaps with the base pattern in a plan view, wherein a plurality of second spacers (under region 32) formed on the main surface of the first substrate and arranged above a part where is between neighboring pixel regions and doe not overlap with the base pattern in a plan view, wherein each of the second spacers is ordinarily spaced from a stacked structure formed on the second

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substrate to accommodate the liquid crystal layer therebetween, and each of the first spacers ordinarily contacts directly the stacked structure formed on the second substrate.

Regarding claim 14, Sumida discloses each of the second spacers contacts with the stacked structure formed on the second substrate, when the first spacers are subjected to an external force and elastically deformed.

Regarding claim 15, Sumida discloses the base pattern is covered by a protective film 5 provided between the base pattern and the first spacers.

Claim Rejections - 35 USC § 103

- 8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Sumida.

Suzuki discloses the device structure as recited in the claim, but does not specifically teach first spacers overlapping intersecting position of first and second signal lines or second spacers contacting a stacked structure which includes first signal line lines but excludes any one of the second signal lines.

Sumida discloses in fig. 2 each of first spacers 7 contacting with a stacked structure at an overlapping intersecting position of one of the first and second signal lines and one of the second signal lines, and second spacers (under region 32) contacting with another part of the stacked

structure which includes one of the first signal lines but excludes any one of the second signal lines (excludes gate line).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify Suzuki's device by incorporating Sumida's teaching since that would improve the cell gap accuracy as taught by Sumida.

Response to Arguments

Applicant's arguments filed 9/1/2005 have been fully considered but they are not persuasive. In response to Applicants argument that Sumida's second spacer is located in the pixel region 82, it is noted that the limitation "between neighboring pixel regions" has a different meaning than "between adjacent pixel regions" and since claims must be "given the broadest reasonable interpretation consistent with the specification" (see MPEP 211), the limitation is met by Sumida's reference.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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November 4, 2005

NATHAN J. FLYNN SUPERVISORY PATENT EXAMINER

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